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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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VEDDER PRICE KAUFMAN & KAMMHOLZ
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EXAMINER

HOYE, MICHAEL W

ART UNIT PAPER NUMBER

2614

DATE MAILED: 12/19/2003

13

Please find below and/or attached an Office communication concerning this application or proceeding.

TS

Office Action Summary

Application No.

09/398,913

Applicant(s)

KLEBANOV ET AL.

Examiner

Michael W. Hoye

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 2-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 2-13, 22 and 23 is/are allowed.
- 6) ☒ Claim(s) 14-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 February 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 14-21 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheney et al (USPN 6,519,283), in view of Adams et al (USPN 6,108,042), both cited by the Examiner.

As to claim 14, note the Cheney et al reference which discloses a method of receiving video graphics data. The claimed receiving a "transport stream associated with a digital video broadcast signal" is met by either of the digital video from cable or satellite 101 (Fig. 4) received at NIM 102, or the signals 104 received at the DMSD 105 (see col. 6, line 35 – col. 7, line 27). The claimed "transport stream having data signals and control signals" is met by the video stream having pixel data signals and synchronization (or control) signals (col. 4, lines 40 and 55-57). The claimed generating a secondary set of control signals...is met by the frame buffer pointer control 686 in Fig. 6, which generates additional control signals from the MPEG or transport stream's control signals. The claimed storing at least a portion of the transport stream

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data signals in a memory buffer controlled by the secondary set of control signals is met by the frame buffer pointer control 686 controlling the rotation of the frame buffers (see col. 10, lines 37-41). Although the Cheney reference discloses a PCI bus 42 (Fig. 2), the Cheney reference does not explicitly disclose the claimed sending the contents of the memory buffer to a system bus. The Adams et al reference teaches a Graphics Display Subsystem 56 in Fig. 2, which includes a frame buffer (col. 5, lines 41-43), that may send information to the system bus 51. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have combined the method of receiving video graphics data as disclosed by the Cheney et al reference with the teachings the Adams et al reference which discloses using a system bus in conjunction with the frame buffer memory for the advantage of having the ability to receive various types of television broadcasts through a computer system with a video graphics adapter and bus type system. One of ordinary skill in the art would have been led to make such a modification since television receivers used with computers are well known in the art to provide additional capabilities within a computer system.

As to claim 15, the Cheney reference discloses multiple modes of operation and a method of receiving a digital video signal that is of a different type than the transport stream, which is met by the video signals received at 104 in Fig. 4 (col. 4, lines 40-42 & 54-57 and col. 6, lines 62-67). The Cheney reference discloses a first mode of operation as shown by receiving a digital video signal 101, which includes a MPEG transport stream (col. 6, lines 37-44). The Cheney reference also discloses another mode of operation where a digital video signal that is of a different type than the transport stream, which is met by the video signals received at 104 in Fig. 4 (col. 4, lines 40-42 & 54-57 and col. 6, lines 62-67) which includes data signals including pixel

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data signals and control signals which are met by the corresponding synchronization signals (col. 4, lines 56-57) and by “pixel select control” signals (col. 7, lines 40-41). The digital multi-standard decoder (DMSD) 105 provides synchronization signals, such as, horizontal sync and vertical sync and in addition, the memory controller 52 in Fig. 2 generates control signals to the DRAM 53 for storing video data in the frame buffer (col. 5, line 54 – col. 6, line 5).

As to claim 16, the Cheney reference as combined above, further discloses a camcorder or television camera may be used as an uncompressed signal and connected video cameras may inherently comprise the transmission of a zoom video signal (see col. 8, lines 24-25 and ZV port definition from the Microsoft Computer Dictionary, p. 586).

As to claim 17, the Cheney et al reference also discloses a method wherein the memory buffer is a frame buffer as shown in Fig. 2, DRAM 53 (col. 5, lines 65-67) and Fig. 6, element 653.

4. Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reitmeier (USPN 6,118,498), in view of Schindler et al (USPN 5,900,867), both cited by the Examiner.

As to claim 18, the Reitmeier reference discloses in Figure 1 a system for receiving a digital video broadcast signal. The claimed “tuner to receive a digital broadcast signal and to provide an analog output signal” is met by tuner 10A or 10B which receives an RF signal, which may include a digital video broadcast (DVB) signal, and provides an analog or intermediate frequency (IF) output (see col. 3, lines 33-57 and col. 2, lines 15-21). The claimed “demodulator coupled to...the tuner, and to provide a transport stream” is met by demodulator 15A or 15B which produce a MPEG or transport stream (see Fig. 1 and col. 3, lines 33-57). Reitmeier

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discloses a transport demultiplexer 35, a video decoder 45, and a format converter 50, which receive the transport stream and are all coupled to the controller 70 through the I/O port 72 (see col. 4, lines 50-67 and col. 2, line 64 – col. 3, line 3). The claimed “video graphics adapter” coupled to receive the transport stream is met in part by the format converter 50, which receives the transport stream V4 and/or V2 (Fig. 1), and has a system interface port F, which connects to controller 70 through I/O port 72. The claimed “video engine” and “output port” are met by the VOUT and video driver (see Fig. 1 (not completely shown) and col. 4, lines 57-60). Reitmeier does not explicitly use the term “video graphics adapter”, however, the Schindler et al reference teaches a VGA type adapter used with a computer system 118, which has a television receiver 316 and PCI Bus 312 (see Figures 1 and 3-5). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have combined the format conversion system for receiving a DVB as disclosed by Reitmeier with the television receiver system for use in a computer as disclosed by Schindler et al for the advantage of having the ability to receive various types of television broadcasts through a computer system with a video graphics adapter and PCI bus type system. One of ordinary skill in the art would have been led to make such a modification since television receivers used with computers are well known in the art to provide additional capabilities within a computer system.

As to claim 19, the Reitmeier reference further discloses in Figure 1 a frame buffer 55 or “memory” to store at least a portion of the MPEG or transport stream (see col. 4, lines 50-67).

As to claim 20, the Reitmeier reference further discloses in Figure 1 a central processing unit 74, which is a part of controller 70 and is coupled the claimed “system interface port” as met

by I/O 72 as described above, and the claimed “transport demultiplexer” coupled to the demodulator is met by transport demultiplexer 35 in Fig. 1 as described above in claim 18.

5. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cheney et al (USPN 6,519,283), in view of Malladi et al (USPN 5,912,676), and in further view of Datari (USPN 6,418,169), all cited by the Examiner.

As to claim 21, note the Cheney et al reference which discloses an integrated video processing system and method of storing video data. Cheney et al discloses multiple modes of operation (see col. 7, lines 27-37, col. 8, line 65 – col. 9, line 8 & lines 15-30). The claimed first mode of operation comprising storing pixel information in a frame buffer of a video adapter, wherein one line of frame buffer memory is representative of one line of a video image to be displayed is met by receiving an uncompressed signal from a second video source which may comprise either a digital signal or an analog signal (col. 6, lines 51-67 and/or 104 in Fig. 4), the pixel data (col. 4, lines 40-42 & 54-57 & col. 6, lines 26-34) is fetched and written to FIFO buffers and placed into frame buffers of the DRAM 52 in Fig. 2 (col. 5, line 52 – col. 6, line 6) and in one mode the uncompressed video is sent to a display. Although, Cheney does not explicitly disclose that one line of the frame buffer memory is representative of a line of video image to be displayed, it is well known in the art of uncompressed video frame buffers that a line of frame buffer memory is *representative* of a line of a video image to be displayed. The Malladi et al reference teaches that various frame storage formats exist for storing frame data in memory, and that one method for storing a frame of pixel data is on a scan line basis, where the data is stored in memory scan line by scan line for pictures or frames that are to be displayed (see

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col. 4, lines 30-37). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the method of Cheney et al which discloses multiple modes of operation for storing video data, with the Malladi et al reference, which specifically teaches that one line of frame buffer memory may be representative of one line of a video image to be displayed for the advantage of providing a storage format which provides improved performance for storing a reference frame of pixel data on a scan line basis. The claimed second mode of operation comprising storing compressed transport stream data in the frame buffer, wherein one line of frame buffer memory is representative of one transport stream packet is met by receiving an MPEG transport stream from a digital video source 101 in Fig 4 (col. 6, lines 35-44), the compressed MPEG transport steam (col. 5, lines 41-44) is sent from transport 103 to PCI bus 42/video decoder 106 (Figs. 2 & 4.) and is fetched and written to video FIFO buffer and placed into frame buffers of the DRAM 52 in Fig. 2 through memory controller 52 (col. 5, line 52 – col. 6, line 6) and in another mode of operation the video is decompressed and sent to a display. Although, Cheney does not explicitly disclose that one line of the frame buffer memory is representative of one transport stream packet, it is well known in the art of video transport streams that are stored in frame buffers that a MPEG-2 transport stream packet has a fixed 188 byte length as defined by MPEG standards, and therefore, a line of frame buffer memory is *representative* of a transport stream packet since every MPEG-2 transport stream packet has already been produced and transmitted according to the established MPEG standards so that when received by a frame buffer memory a line of memory is representative of one transport stream packet. In addition to, the Datari reference teaches that MPEG video data packets may be stored or buffered in memory and sequentially accessed by priority (see col. 5,

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lines 25-42 and col. 6, lines 62-66). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further combined the method of Cheney et al which discloses multiple modes of operation for storing video data, with the Datari reference, which specifically teaches that a line of the frame buffer memory may be representative of one MPEG or transport stream packet for the advantage of providing a storage format which allows for improved priority accessing of transport stream packets of video images to be displayed.

Allowable Subject Matter

6. Claims 2-13 and 22-23 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

As to claim 22, the prior art, alone or in combination, does not teach or fairly suggest a video graphics system comprising a data storage controller having at least one pair of a plurality of internal control ports to communicate control signals within the data storage controller.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ristau (USPN 5,949,441) – Discloses frame buffer memory with packet storage and line storage.

Hoogenboom (USPN 5,717,461) – Discloses frame buffer storage accommodating to video lines.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael W. Hoyer whose telephone number is (703) 305-6954.

The examiner can normally be reached on Monday to Friday from 8:30 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller, can be reached at (703) 305-4795.

Any response to this action should be mailed to:

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to customer service whose telephone number is **(703) 308-HELP**.

Michael W. Hoyer
December 2, 2003


JOHN MILLER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600